CLAIMS

1 A system comprising:

a bus;

at least one master configured to present at least one transfer signal; and

a first circuit coupled between said bus and said at least one master, said first circuit configured to (i) grant a bus mastership to a first master of said at least one master, (ii) present a first transfer signal of said at least one transfer signal to said bus in response to granting said bus mastership to said first master, (iii) remove said bus mastership from all masters of said at least one master, and (iv) present an idle transfer signal to said bus in response to removing said bus mastership from said all masters.

2. The system according to claim 1, wherein (i) said first circuit is further configured to detect when zero masters of said at least one master are able to use said bus and (ii) removing said bus mastership from said all masters is done in response to detecting when said zero masters are able to use said bus.

3. The system according to claim 2, wherein detecting when said zero masters are able to use said bus is detecting when each of said at least one master is simultaneously involved in a split response.

4. The system according to claim 2, wherein detecting when said zero masters are able to use said bus is detecting when said first master has locked said bus mastership and said first master is involved in a split response.

5. The system according to claim 2, wherein detecting when said zero masters are able to use said bus is detecting when said first master is involved in a split response and no other masters of said at least one master is requesting said bus mastership.

6. The system according to claim 2, wherein detecting when said zero masters are able to use said bus is detecting when none of said at least one master is requesting said bus mastership.

7. The system according to claim 1,wherein said at least one master is a plurality of masters.

8. The system according to claim 7, wherein said first circuit comprises:

an arbiter configured to present a master signal identifying said first master of said plurality of masters; and

a second circuit configured to multiplex a plurality of said at least one transfer signals received from said plurality of masters responsive to said master signal to present said first transfer signal to said bus.

9. The system according to claim 8, wherein (i) said arbiter is further configured to present a control signal and (ii) said second circuit is further configured to present one of said first transfer signal and said idle transfer signal to said bus responsive to said control signal.

10. The system according to claim 9, wherein said first circuit is further configured to detect when (i)(a) said all masters are simultaneously involved in a split response, (i)(b)

said first master has locked said bus mastership and is involved in a split response, (i)(c) said first master is involved in said split response an no other master of said at least one master is requesting said bus mastership, and (i)(d) none of said at least one master is requesting said bus mastership, and (ii) removing said bus mastership from said all masters is performed in response to detecting at least one of (i)(a), (i)(b), (i)(c) and (i)(d).

11. A method of operating a bus comprising the steps of:

(A) granting a bus mastership to a first master of at least one master;

(B) presenting a first transfer signal of at least one transfer signal from said first master to said bus in response to step (A);

(C) removing said bus mastership from all masters of said at least one master; and

(D) presenting an idle transfer signal to said bus in response to step (C).

12. The method according to claim 11, further comprising the step of detecting when zero masters of said at least one master are able to use said bus, wherein said removing said bus mastership of step (A) is performed in response to detecting said zero masters are able to use said bus.

13. The method according to claim 12, wherein said detecting when said zero masters are able to use said bus is detecting when said all masters are simultaneously involved in a split response.

14. The method according to claim 12, wherein said detecting when said zero masters are able to use said bus is detecting when said first master has locked said bus mastership and is involved in a split response.

15. The method according to claim 12, wherein said detecting when said zero masters are able to use said bus is detecting when said first master is involved in a split response and no other master of said at least one master is requesting said bus mastership.

16. The method according to claim 12, wherein said detecting when said zero masters are able to use said bus is detecting when none of said at least one master is requesting said bus mastership.

17. The method according to claim 11, wherein said at least one master is a plurality of masters, the method further comprising the steps of:

presenting a master signal identifying said first master of said plurality of masters;

multiplexing a plurality of said at least one transfer signals received from said plurality of masters in response to said master signal; and

presenting said first transfer signal to said bus in response to multiplexing said plurality of said transfer signals.

18. The method according to claim 17, further comprising the steps of:

presenting a control signal; and

presenting one of said first transfer signal and said idle transfer signal to said bus in response to said control signal.

19. The method according to claim 17, further comprising the steps of:

multiplexing said plurality of said at least one transfer signals in response to said master signal;

presenting said first signal in response to multiplexing said plurality of said at least one transfer signals;

generating said idle transfer signal; and

presenting one of said idle transfer signal and said first transfer signal to said bus in response to said control signal.

20. A system comprising:

means for granting a bus mastership to a first master of at least one master;

means for presenting a first transfer signal of at least one transfer signal from said first master to said bus in response to granting said bus mastership to said first master;

means for removing said bus mastership from all masters of said at least one master; and

means for presenting an idle transfer signal to said bus in response to removing said bus mastership from said all masters.